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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,672	AASHEIM ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication filed on July 27, 2005. This amendment has been entered and carefully considered. Claims 1-44 are again presented for examination.

2. Applicant's arguments filed on July 27, 2005 have been fully considered but they are not deemed to be persuasive.

3. The rejection of claims 1-7, 9-14, 16-29, 31-37 and 39-44 as in the previous Office Action is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5-7, 9-11, 16-17, 22-25, 29, 31-33, 37, 39 and 40-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Ban (USPN: 5,799,168).

As per claim 1, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising a flash memory driver (the standardized flash controller in Fig. 1) that is executable by a computer to interface between a file system and one or more flash memory media, the

flash memory driver comprising: flash abstraction logic (i.e. the group of interfaces/controllers, between the CPU and the flash memory) and invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media (e.g. see Col. 2, lines 36-38); and flash media logic (a simple discrete logic or interface) configured to interact with different types of the flash memory media (any flash chip); wherein the flash abstraction logic invokes the flash media logic to perform memory operations (generic commands) that are potentially performed in different ways depending on the type of the flash memory media (e.g. see the abstract, Col. 2, lines 36-48; Col. 4, lines 33-39, 61-65 and claim 2).

As per claims 5 and 6, Ban teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein one of the flash memory operations includes mapping status information associated with physical sectors of the flash memory medium for use by the file system, i.e. translating commands from/to physical sectors of the flash memory medium to/from commands for used in the file system (CPU) (e.g. see Col. 5, lines 29-37).

As per claim 7, Ban teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein the flash medium logic (simple discrete logic) is a user programmable to read, write and erase data to and from the flash memory medium (e.g. see Col. 3, line 49 – Col. 4, line 13).

As per claim 17, Ban teaches the claimed invention as described above and furthermore, Ban teaches that the flash abstraction logic that is interface/controller, between the CPU and the flash memory, passes specific commands associated with

certain types of flash memory media directly to the flash medium logic (a simple discrete logic or interface) for translation and further execution (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claims 23 and 29, Ban teaches a processing device that uses a flash memory medium for storage of data, comprising: a file system (the flash file system), configured to control data storage for the processing device (i.e. the CPU in Fig. 1) (e.g. see Col. 2, lines 17-23); flash media logic (a simple discrete logic or interface which comprises the command register) configured to perform physical sector operations to a flash memory medium based on physical sector commands, wherein the flash medium logic comprises a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected (e.g. see Col. 3, lines 15-24); and flash abstraction logic that is interface/controller, between the CPU and the flash memory, configured to maintain flash memory requirements, which are common to a plurality of different flash memory media, that are necessary to operate the flash memory medium (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claim 40, Ban teaches the claimed invention as described above and furthermore, Ban teaches that the method further comprises receiving read and write commands from a file system that is inherently embedded in the controller taught by Ban (e.g. see Col. 1, lines 35-39 and Col. 2, lines 40-44).

As per claim 41, Ban teaches the claimed invention as described above and furthermore, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising computer-

executable instructions (commands stored in the command register) that, when executed, perform the method as taught by Ban (e.g. see Col. 3, lines 15-24 and Fig. 1).

Claims 9, 18, 25 and 42-43 are rejected based on the same rationale as the rejection of claim 1.

Claims 11, 31 and 37 are rejected based on the same rationale as the rejection of claim 6.

Claims 10, 22, 32, 39 and 44 are rejected based on the same rationale as the rejection of claim 7.

Claim 16 is rejected based on the same rationale as the rejection of claims 1 and 7.

Claim 24 is rejected based on the same rationale as the rejection of claims 17.

Claim 33 is rejected based on the same rationale as the rejection of claims 16 and 17.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 12, 20, 27 and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Bruce et al. (USPN: 6,000,006) hereinafter, Bruce.

As per claim 2, Ban teaches the claimed invention as described above. However, Ban failed to teach that one of the flash memory operations includes performing wear-leveling operations associated with the flash memory medium. Bruce, on the other hand, teaches that the benefits of using a unified re-mapping and wear-leveling table overcome the disadvantages of the larger granularity of block re-mapping. As flash-memory sizes increase, the relative loss from block rather than page re-mapping decreases (e.g. see Col. 10, lines 7-15). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Bruce in the flash memory driver taught by Ban to recognize the benefits as stated above.

Claims 12, 20, 27 and 35 are rejected based on the same rationale as the rejection of claim 2.

6. Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Martwick (USPN: 6,493,807).

As per claims 3 and 4, Ban teaches the claimed invention as described above. However, Ban failed to teach that one of the flash memory operations includes maintaining data integrity of the flash memory medium and handling recovery of data associated with the flash memory medium after a power-failure. Martwick, on the other hand, teaches the method for updating the flash blocks so the data integrity gets maintained and the data can be recovered upon a power failure (e.g. see Col. 3, lines 37-39). Accordingly, it would have been obvious to one of ordinary skill in the art at the

time of the current invention was made to implement the method of updating the flash blocks as taught by Martwick in the Ban's flash memory driver to recognize the benefits as stated above.

Claims 13-14, 19, 21, 26, 28, 34 and 36 are rejected based on the same rationale as the rejection of claims 3 and 4.

Remarks

7. As to the remark, Applicant asserted:

(a) Ban fails to disclose "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media" as recited in claim 1 because the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips.

(b) The controllers of Ban are ill-equipped "to interact with different types of the flash memory media".

(c) Ban fails to disclose "wherein the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media". Rather, under Ban the controllers are bound to a particular flash chip and thus are limited to performing memory operations specific to that flash chip.

(d) Ban teaches away from the flash memory driver and flash medium logic disclosed in claim 6, by requiring the CPU – rather than the flash driver – to

coordinate and organize all mappings between a computer's memory and a flash array.

(e) Ban also fails to disclose "wherein the flash medium logic is further configured to translate commands received from the file system to physical sector commands for issuance to the flash memory media" as recited in claim 6.

(f) Ban fails to teach the flash driver of claims 9 and 16.

(g) Ban fail to disclose or show "user programmable flash medium logic, configured to read, write and erase data to and from flash memory medium".

(h) Ban fails to disclose the processing device of claims 23 and 33.

(i) Ban does not disclose "issuing physical sector commands directly to the flash memory medium from a flash medium logic".

(j) A single controller under Ban cannot provide an interface between "one of a plurality of different flash memory media" as disclosed in claims 42-43.

(k) Under Ban no one controller can interface with a flash memory medium, selected from one of a plurality of different flash memory media, and no one controller can manage a set of characteristics common to a plurality of different flash memory media at a flash abstraction logic.

(l) There is no disclosure in Ban which mentions "programmable entry points that can be optionally selected by a user".

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a) and (b), in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the controllers used under Ban are flash chip specific, and cannot be used with other types of flash chips" and "controllers of Ban are ill-equipped to interact with different types of the flash memory chips") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The rejected claims states "flash abstraction logic that is invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media and flash media logic configured to interact with different types of the flash memory media". The flash abstraction logic is taught by Ban as the group of interfaces/controllers, between the CPU and the flash memories and the flash media logic is taught by Ban as the simple discrete logic/interface (e.g. see Col. 4, lines 33-39, 61-65 and Fig. 1).

With respect to (c), as stated above the flash abstraction logic is taught by Ban as the group of interfaces/controllers between the CPU and the flash memories instead of one specific controller (e.g. see Col. 4, lines 33-39, 61-65 and Fig. 1). Therefore, Ban does teach that the flash abstraction logic, i.e. the group of interfaces/controllers between the CPU and the flash memories, invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media, i.e. the specific controller would be used from the group of controllers depending on the type of the flash memory media.

With respect to (d) and (e), Examiner respectfully disagrees with Applicant's argument because Ban clearly teaches about translating commands received from the CPU, i.e. the file system, into commands specific to the type of the flash chip present, i.e. the physical sector commands, by the standardized controller translating apparatus – not by the CPU as stated by the Applicant -- (e.g. see Col. 5, lines 30-35). The further limitation of "organize all mappings between a computer's memory and a flash array" upon which the Applicant relies is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

With respect to (f), Ban clearly teaches about translating commands received from the CPU, i.e. the file system, into commands specific to the type of the flash chip present, i.e. the physical sector commands, by the standardized controller translating apparatus – not by the CPU as stated by the Applicant -- (e.g. see Col. 5, lines 30-35). Ban teaches that the flash abstraction logic (i.e. the group of interfaces/controllers, between the CPU and the flash memory medium) configured to map a logical sector status from the file system to a physical sector status of the flash memory medium (e.g. see Col. 5, lines 30-35); and maintain memory requirements associated with operating the flash medium (e.g. see Col. 4, lines 33-39, 61-65).

With respect to (g), as recited in the rejection of claim 7 above, Ban clearly teaches the flash memory driver, wherein the flash medium logic is a user

programmable to read, write and erase data to and from the flash memory medium (e.g. see Col. 3, line 49 – Col. 4, line 13).

With respect to (h), Ban does teach the processing device (i.e. CPU in Fig. 1) as claimed in claims 23 and 33.

With respect to (i), Ban does teach about issuing physical sector commands directly to the flash memory medium (array of flash chips) from a flash medium logic (array of flash controllers) (e.g. see Fig. 2).

With respect to (j) and (k), Examiner agreed with the Applicant that a single controller cannot provide an interface between one of a plurality of different flash memory media, however, Examiner would like to point out that the flash driver is (compared with) a group of interfaces/controllers between the CPU and the flash memories taught by Ban. And, Ban does teach that a flash driver (a group of interfaces/controllers between the CPU and the flash memories) which provides an interface between a file system (CPU) and a flash memory medium (flash chips) (e.g. see Fig. 2).

With respect to (l), Ban teaches that the flash medium logic (simple discrete logic) is a user programmable to read, write and erase data to and from the flash memory medium, i.e. comprises programmable entry points that can be optionally selected by a user to read, write or erase the data (e.g. see Col. 3, line 49 – Col. 4, line 13).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER